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AMENDMENTS IN THE CLAIMS:

1. (Currently Amended) A system in a media access controller in a data link layer for communicating to a number of physical layer devices in a physical layer, comprising:

a common bus port for electrical coupling to a common bus that is electrically coupled to the physical layer devices, the common bus serving as a direct interface between the data link layer and the physical layer;

logical circuitry to transmit a training sequence from the common bus port to the physical layer devices; and

logical circuitry to transmit a data block from the common bus port to a respective one of the physical layer devices by way of the common bus, the data block being transmitted in one of a number of time slots of a time division multiplexed transmission.

2. (Original) The system of claim 1, wherein the logical circuitry to transmit a training sequence from the common bus port further comprises logical circuitry to transmit a transmit enable signal from the common bus port simultaneously with the data block, thereby indicating a transmission of the data block to the physical layer devices.

3. (Original) The system of claim 1, wherein the logical circuitry to transmit a training sequence from the common bus port to the physical layer devices further comprises logical circuitry to transmit an address designation in each of the time slots.

4. (Original) The system of claim 1, wherein the logical circuitry to transmit a training sequence from the common bus port to the physical layer devices further comprises logical circuitry to transmit a predefined training sequence that provides a reference for the time slots.

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5. (Original) The system of claim 3, wherein each of the address designations is transmitted in a first portion of the corresponding time slot.

6. (Original) The system of claim 5, wherein a predetermined sequence is transmitted in a second portion of the corresponding time slot.

7. (Currently Amended) A system in a media access controller in a data link layer for communicating to a number of physical layer devices in a physical layer, comprising:

a processor coupled to a local interface;

a memory coupled to the local interface;

a common bus port coupled to the local interface, the common bus port being adapted for electrical coupling to a common bus that is electrically coupled to the number of physical layer devices, the common bus serving as a direct interface between the data link layer and the physical layer; and

operating logic stored on the memory and executable by the processor, the operating logic further comprising:

logic to transmit a training sequence from the common bus port to the physical layer devices; and

logic to transmit a data block from the common bus port to a respective one of the physical layer devices by way of the common bus, the data block being transmitted in one of a number of time slots of a time division multiplexed (TDM) transmission.

8. (Original) The system of claim 7, wherein the logic to transmit a training sequence from the common bus port to the physical layer devices further comprises logic to transmit a transmit enable signal from the common bus port simultaneously with the data block, thereby indicating a transmission of the data block to the physical layer devices.

9. (Original) The system of claim 7, wherein the logic to transmit a training sequence from the common bus port to the physical layer devices further comprises logic to transmit an address designation in each of the time slots.

10. (Original) The system of claim 7, wherein the logic to transmit a training sequence from the common bus port to the physical layer devices further comprises logic to transmit a predefined training sequence that provides a reference for the time slots.

11. (Original) The system of claim 10, wherein each of the address designations is transmitted in a first portion of the corresponding time slot.

12. (Original) The system of claim 10, wherein a predetermined sequence is transmitted in a second portion of the corresponding time slot.

13. (Currently Amended) A system in a media access controller in a data link layer for communicating to a number of physical layer devices in a physical layer, comprising:

a common bus port coupled to the local interface, the common bus port being adapted for electrical coupling to a common bus that is electrically coupled to the number of physical layer devices, the common bus serving as a direct interface between the data link layer and the physical layer;

means for transmitting a training sequence from the common bus port to the physical layer devices; and

means for transmitting a data block from the common bus port to a respective one of the physical layer devices by way of the common bus, the data block being transmitted in one of a number of time slots of a time division multiplexed (TDM) transmission.

14. (Original) The system of claim 13, wherein the means for transmitting a training sequence from the common bus port to the physical layer devices further comprises means for transmitting a transmit enable signal from the common bus port simultaneously with the data block, thereby indicating a transmission of the data block to the physical layer devices.

15. (Original) The system of claim 13, wherein the means for transmitting a training sequence from the common bus port to the physical layer devices further comprises means for transmitting an address designation in each of the time slots.

16. (Currently Amended) A method in a media access controller in a data link layer for communicating to a number of physical layer devices in a physical layer, comprising the steps of:

transmitting a training sequence to the physical layer devices by way of a common bus, the common bus serving as a direct interface between the data link layer and the physical layer; and

transmitting a data block to a respective one of the physical layer devices by way of the common bus, the data block being transmitted in one of a number of time slots of a time division multiplexed (TDM) transmission.

17. (Original) The method of claim 16, wherein the step of transmitting a training sequence to the physical layer devices by way of a common bus further comprises the step of transmitting a transmit enable signal to the physical layer devices by way of the common bus simultaneously with the transmission of the data block, thereby indicating a transmission of the data block to the physical layer devices.

18. (Original) The method of claim 16, wherein the step of transmitting a training sequence to the physical layer devices by way of a common bus further comprises the step of transmitting an address designation in each of the time slots.

19. (Withdrawn) A system in a physical layer device to receive data from a media access controller, comprising:

a common bus input port for electrical coupling to a common bus that is electrically coupled to a number of physical layer devices and the media access controller;

logical circuitry to maintain an address designation associated with the physical layer device;

logical circuitry to synchronize with a time slot dedicated to the physical layer device, the time slot appearing in a time division multiplexed transmission received through the common bus port; and

logical circuitry to receive a data block transmitted through the time slot.

20. (Withdrawn) The system of claim 19, further comprising logical circuitry to receive a transmit enable signal through the common bus port that indicates a transmission of the data block in the time slot, thereby causing the execution of the logic to receive the data block.

21. (Withdrawn) The system of claim 19, wherein the logical circuitry to synchronize with a time slot dedicated to the physical layer device further comprises logical circuitry to compare the address designation with an address block transmitted in the time slot to determine a match there between.

22. (Withdrawn) A system in a physical layer device to receive data from a media access controller, comprising:

a processor coupled to a local interface;

a memory coupled to the local interface;

a common bus input port for electrical coupling to a common bus that is electrically coupled to a number of physical layer devices and the media access controller; and

operating logic stored on the memory and executable by the processor, the operating logic further comprising:

logic to maintain an address designation associated with the physical layer device;

logic to synchronize with a time slot dedicated to the physical layer device, the time slot appearing in a time division multiplexed transmission received through the common bus port; and

logic to receive a data block transmitted through the time slot.

23. (Withdrawn) The system of claim 22, wherein the operating logic further comprises logic to receive a transmit enable signal through the common bus port that indicates a transmission of the data block in the time slot, thereby causing the execution of the logic to receive the data block.

24. (Withdrawn) The system of claim 22, wherein the logic to synchronize with a time slot dedicated to the physical layer device further comprises logic to compare the address designation with an address block transmitted in the time slot to determine a match there between.

25. (Withdrawn) A system in a physical layer device to receive data from a media access controller, comprising:

means for maintaining an address designation associated with the physical layer device;

means for synchronizing with a time slot dedicated to the physical layer device, the time slot appearing in a time division multiplexed transmission received through the common bus port; and

means for receiving a data block transmitted through the time slot.

26. (Withdrawn) A method in a physical layer device to receive data from a media access controller, comprising the steps of:

maintaining an address designation associated with the physical layer device;

synchronizing with a time slot dedicated to the physical layer device, the time slot appearing in a time division multiplexed transmission received through the common bus port; and

receiving a data block transmitted through the time slot.